(A) AMENDMENT OF THE CLAIMS:

1. (Currently Amended) A logic synthesis method for reducing the delay of a timing critical path in a circuit, comprising the steps of:

(a) selecting a gate which is not an inverter in the timing critical path [[,]];

(b) swapping said timing critical path to a pin of said gate [[,]];

(c) replacing said gate with a functionally equivalent tapered gate [[,]];

(d) performing a timing analysis of said circuit [[,]]; and

(e) if said timing analysis of said circuit indicates improvement in a worst case delay through said circuit [[,]];

(f) then retaining said tapered gate, and

(g) if said timing analysis of said circuit indicates no improvement in said worst case delay through said circuit [[,]];

(h) then swapping said tapered gate back to said selected gate for use in said circuit.

2. (Currently Amended) The logic synthesis method of claim 1 , wherein

said gate is selected from a gate library comprising a set of non-tapered gates and a set of tapered gates, and wherein in said gate library,
said non-tapered gates are characterized by a stack of devices of the same width and said tapered gates are characterized by a stack of devices of different widths.

3. (Currently Amended) The logic synthesis method of claim 1 , wherein said gate is selected from a gate library comprising a set of non-tapered gates and a set of tapered gates,
and wherein each set in said gate library comprises one or more of the following gates: NAND gates, NOR gates, AND-OR-INVERT gates, and OR-AND-INVERT gates.

4. (Currently Amended) A logic synthesis method as in claim 3 , whereby the delay through said tapered gate and the delay through said non-tapered gate are compared.

[[6.]] 5. (Currently Amended) A logic synthesis method as in claim 1 , whereby a plurality of tapered gates exist for a non-tapered gate, said plurality of tapered gates being functionally equivalent to said non-tapered gate.

[[7.]] 6. (Currently Amended) A logic synthesis method as in claim [[6]] 5, whereby the selection of said plurality of tapered gates available for use in said circuit is swapped into said circuit for comparison with a timing analysis of the circuit.

[[8.]] 7. (Currently Amended) A logic synthesis method as in claim [[7]] 6, whereby the delay through said plurality of

tapered gates and the delay through said non-tapered gate are compared.

[[9.]] 8. (Currently Amended) A logic synthesis method as in claim [[8]] 7, whereby the gate of said plurality of gates which yields the shortest delay is the one retained for said circuit.